CLAIMS

What is claimed is:

1. A high-speed interconnection adapter that comprises:

a first-in-first-out (FIFO) buffer for each of a plurality of channels; and

a reconstruction logic coupled to the FIFO buffers and configured to monitor output symbols in the FIFO buffers for start symbols, wherein upon detection of a start symbol from less than all the FIFO buffers the reconstruction logic is configured to suspend output from the FIFO buffers in which start symbols were detected, wherein the suspension continues until start symbols are detected in all FIFO buffers.

2. The adapter of claim 1, wherein once start symbols are detected in all FIFO buffers the reconstruction logic is configured to retrieve symbol groups in sequence from the FIFO buffers, each symbol group consisting of one symbol from each FIFO buffer.

3. The adapter of claim 2, wherein the reconstruction logic is configured to form a symbol sequence by ordering symbols with the symbol groups and concatenating the symbol groups which represent data.

4. The adapter of claim 3, wherein the symbols are eight-bit bytes.

5. The adapter of claim 3, wherein comma symbol groups and skip symbol groups do not represent data.

6. The adapter of claim 1, wherein the start symbol is a comma symbol.

7. The adapter of claim 1, the suspension is limited to less than a predetermined number of symbol periods, and wherein if start symbols are not detected in all FIFO buffers at the end of the predetermined number of symbol periods, the FIFO buffers are cleared and the suspension is lifted.

8. The adapter of claim 7, wherein the predetermined number of symbol periods is less than half of the number of symbol periods in a training sequence.

9. The adapter of claim 7, wherein the predetermined number of symbol periods is one-fourth of the number of symbol periods in a training sequence.

10. The adapter of claim 1, further comprising:

a channel decoder for each of the plurality of channels configured to provide symbols to the FIFO buffers, wherein the channels are independent serial channels, and wherein the channel decoder is an 8B/10B code decoder.

11. A method of de-skewing data received via a plurality of channels, wherein the method comprises:

receiving symbols into a plurality of FIFO buffers that corresponds to a respective plurality of communication channels;

for each FIFO buffer, removing symbols until a start symbol is detected;

upon detection of one or more start symbols from less than all of the plurality of FIFO buffers, suspending removal from those FIFO buffers in which a start symbol is detected.

12. The method of claim 11, wherein said suspending lasts for a maximum number of symbol periods unless start symbols are detected in all the FIFO buffers.

13. The method of claim 12, wherein the maximum number is less than half of a predetermined number of symbol periods in a training sequence.

14. The method of claim 11, further comprising:

upon detection of start symbols in all of the plurality of FIFO buffers, retrieving symbol groups in sequence from the FIFO buffers, each symbol group consisting of one symbol from each FIFO buffer.

15. The method of claim 14, further comprising:

combining symbol groups to produce an output symbol sequence.

16. The method of claim 15, wherein said combining includes stripping out demarcation and filler symbols.

17. The method of claim 16, wherein the symbols are eight-bit bytes.

18. A network that comprises:

a communications link comprising multiple independent serial lanes;

a first device having a first network adapter; and

a second device having a second network adapter coupled to the first network adapter via the communications link, wherein the first network adapter is configured to initiate communication by repeatedly transmitting a training sequence that includes a start symbol for each lane and a lane identifier for each lane, and wherein the second network adapter includes:

a set of buffers, each buffer configured to receive training sequence symbols conveyed by a corresponding serial lane; and

a circuit coupled to the buffers and configured to remove symbol groups from the set of buffers until a start symbol is detected, wherein if a start symbol is detected in less than all the buffers, the circuit is configured to remove symbols from only those buffers not having a detected start symbol, this selective removing continuing until all the buffers have a detected start symbol.

19. The network of claim 18, wherein the circuit is configured to clear the set of buffers if the selective removing continues for more than a predetermined number of symbols.